PVP 14

Code: EC5T5

III B.Tech - I Semester – Regular/Supplementary Examinations
March 2021

DIGITAL IC APPLICATIONS

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

PART – A

Answer ***all*** the questions. All questions carry equal marks

11x 2 = 22 M

1. a) What is the difference between initial and always blocks?
   b) Discuss the differences between blocking and non-blocking statements.
   c) Explain the syntax of any two System Tasks with an example.
   d) Compare CMOS and TTL families with respect to any two characteristics.
   e) Define a propagation delay time of a gate.
   f) Draw the logic diagram of IC 74x138.
   g) Write the typical symbols of four Tri state gates.
   h) What is the difference between latch and flip-flop?
   i) What is a race around condition?
   j) Write down the applications of ROM.
   k) What are the advantages of two-dimensional decoding in ROM?

PART – B

Answer any ***THREE*** questions. All questions carry equal marks.

3 x 16 = 48 M

2. a) Discuss different steps of design flow in VLSI. 8 M

   b) Explain the following terms relevant to Verilog HDL. 8 M
   i) Module ii) Test bench

3. a) Discuss the factors to be considered for CMOS/TTL Interfacing. 8 M

   b) Construct a CMOS 4-input AND-OR-INVERT gate and explain its operation with function table. 8 M

4. Illustrate an 8x1 multiplexer and write a behavioral level description along with a test bench and simulation results using Verilog HDL. 16 M

5. a) Design a 4-bit up/down counter and write a behavioral level description using Verilog HDL. 8 M

   b) Write a Verilog code for 4-bit bi-directional shift register using behavior level modeling style. 8 M

6. a) What is a ROM? Explain the internal ROM structure with logic diagram of 8x4 diode ROM. 8 M

   b) Distinguish PROM, EPROM and EEPROM technologies. 8 M